UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,547	11/06/2008	Kouji Tasaki	1204.46479X00	8271
20457 7590 07/19/2010 ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET			EXAMINER	
			TARDIF, DAVID P	
SUITE 1800 ARLINGTON, VA 22209-3873			ART UNIT	PAPER NUMBER
			2876	
			MAIL DATE	DELIVERY MODE
			07/19/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
Office Action Commence	10/588,547	TASAKI ET AL.				
Office Action Summary	Examiner	Art Unit				
	DAVID TARDIF	2876				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1)⊠ Responsive to communication(s) filed on <u>29 A</u>	nril 2010					
·=	, 					
•	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
closed in accordance with the practice under £	x parte Quayle, 1955 C.D. 11, 45	3 O.G. 213.				
Disposition of Claims						
4)⊠ Claim(s) <u>1-15</u> is/are pending in the application.	Claim(s) 1-15 is/are pending in the application.					
4a) Of the above claim(s) is/are withdray	4a) Of the above claim(s) is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-15</u> is/are rejected.	· ··· 					
7) Claim(s) is/are objected to.						
	election requirement					
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9)☐ The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>07 August 2006</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a) ☑ All b) ☐ Some * c) ☐ None of:						
	1. Certified copies of the priority documents have been received.					
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Da					
Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 20100315. 5) Notice of Informal Patent Application 6) Other:						

DETAILED ACTION

This action is responsive to amendments filed 04/29/2010.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 03/15/2010 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 1. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haas et al. (7,015,479) as modified by Morizumi et al. (6,459,588).

As to **claim 1**: Haas et al. teaches an electronic device comprising an IC element (column 3, lines 50-53), and a first circuit layer (50) and second circuit layer (22), wherein the IC element further provides a base substrate (12) formed of silicon (last paragraph, column 2), a semiconductor circuit layer forming a semiconductor

circuit on one side of the base substrate (56), an electrode formed on the semiconductor circuit layer (16), and the other side of the base substrate does not have any electrode formed thereon (figure 1), wherein the first circuit layer is electrically connected to the electrode (column 4, lines 29-31, where the electrode is connected in that it is a FET, and figure 1 shows 30 connected with 50, shown more clearly in figures 2 and 3 as connected).

Haas et al. is silent as to that either circuit layers are connected via a conductive adhesive agent or an anisotropic conductive adhesive agent. Please note that the examiner is reading this limitation in the alternative due to the phrasing "any of the other side of the base substrate and the electrode".

Morizumi et al. teaches that the other side of the base substrate is connected with either the first or the second circuit layer via a conductive adhesive agent (18, figure 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Morizumi et al. with the teachings of Haas et al. so that when pressure is applied in an improper manner, conduction will not occur (last paragraph, column 3).

As to **claim 3**: Morizumi et al. teaches that the conductive adhesive agent is comprised of a thermal hardenable matrix resin (last paragraph, column 5, continuing in column 6), and metallic pieces of granular form (shown in figure 2).

As to **claim 5**: Morizumi et al. teaches that the conductive adhesive agent is comprised of a thermal hardenable matrix resin (last paragraph, column 5, continuing in column 6), and metallic pieces of granular form (shown in figure 2).

As to **claim 6**: Morizumi et al. teaches that the IC element is sealed by a matrix resin of anisotropic conductive adhesive agent (18, figure 3, last paragraph, column 5, continuing in column 6).

As to **claim 7**: Haas et al. as modified by Morizumi et al. teaches the limitations from claim 1.

Haas et al. teaches a conductive circuit layer, but is silent as to that the layer is either aluminum or copper.

Morizumi et al. teaches that at least either the first or the second circuit layers includes a conductive layer of aluminum or copper (column 4, lines 26-44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Haas et al. with the teachings of Morizumi et al. so that the conductive layer will be made of a standard and cheap material that is well known in the art to be conductive.

As to **claim 8**: Haas et al. as modified by Morizumi et al. teaches the limitations of claim 1.

Haas et al. is silent as to that the base substrate be made of an organic resin comprising PET.

Morizumi et al. teaches that the base substrate is comprised of an organic resin being polyethylee terephthalate (column 6, lines 23-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Haas et al. with the teachings of Morizumi et al. so that the substrate will be made of a standard and cheap material that is well known in the art.

As to **claim 9**: Haas et al. as modified by Morizumi et al. teaches the limitations of claim 1.

Haas et al. is silent as to that the base substrate be made of paper.

Morizumi et al. teaches that the base substrate is comprised of paper (lines 45-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Haas et al. with the teachings of Morizumi et al. so that the substrate will be made of a standard and cheap material that is well known in the art.

As to **claim 10**: Morizumi et al. teaches that the IC element is sealed by a matrix resin of anisotropic conductive adhesive agent (18, figure 3, last paragraph, column 5, continuing in column 6).

As to **claim 11**: Haas et al. as modified by Morizumi et al. teaches the limitations from claim 10.

Haas et al. teaches a conductive circuit layer, but is silent as to that the layer is either aluminum or copper.

Morizumi et al. teaches that at least either the first or the second circuit layers includes a conductive layer of aluminum or copper (column 4, lines 26-44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Haas et al. with the teachings of Morizumi et al. so that the conductive layer will be made of a standard and cheap material that is well known in the art to be conductive.

As to **claim 12**: Haas et al. as modified by Morizumi et al. teaches the limitations of claim 11.

Haas et al. is silent as to that the base substrate be made of an organic resin comprising PET.

Morizumi et al. teaches that the base substrate is comprised of an organic resin being polyethylee terephthalate (column 6, lines 23-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Haas et al. with the teachings of Morizumi et al. so that the substrate will be made of a standard and cheap material that is well known in the art.

As to **claim 13**: Haas et al. as modified by Morizumi et al. teaches the limitations of claim 12.

Haas et al. is silent as to that the base substrate be made of paper.

Morizumi et al. teaches that the base substrate is comprised of paper (lines 45-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Haas et al. with the teachings of

Morizumi et al. so that the substrate will be made of a standard and cheap material that is well known in the art.

As to **claim 14**: Haas et al. teaches that one of the circuit layers is an antenna for reception and transmission (22, column 3, lines 38-67 and continuing on column 4 to line 22).

As to **claim 15**: Haas et al. teaches that one of the circuit layers is an antenna for reception and transmission (22, column 3, lines 38-67 and continuing on column 4 to line 22) including a slit (gap seen in figure 1, going from the bottom through 12 to touch 50) and the second circuit layer is a bridging plate electrically connecting the IC element and first circuit layer (figures 1, 2 and 3 show that 50 connects all components of the circuitry).

Response to Amendment

Applicant has amended claim 1 to include the limitations of claim 2, and to further limit the lack of an electrode on an opposite side of a substrate with an electrode formed thereon. Claims 14 and 15 are newly added, explaining an antenna as one of the circuit layers.

Response to Arguments

Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2876

Applicant argues that Morizumi et al. does not teach the lack of an electrode on an opposite side of a substrate with an electrode formed thereon. Examiner agrees, and as is such, has applied rejections in view of Haas et al. as modified by Morizumi et al. Please note that while Haas et al. contains the structure required by the claims, the material components are not specifically detailed in Haas et al., and therefore the examiner relies on Morizumi et al. for these limitations. Examiner does not feel that Morizumi et al. teaches away from the invention in these aspects as Haas et al. teaches the layers of components as taught by the instant application.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Application/Control Number: 10/588,547 Page 9

Art Unit: 2876

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID TARDIF whose telephone number is (571)270-7810 and email is david.tardif@uspto.gov. The examiner can normally be reached on Monday through Friday, 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lee can be reached on (571)272-2398. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DAVID TARDIF/ Examiner, Art Unit 2876

/Michael G Lee/ Supervisory Patent Examiner, Art Unit 2876